



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/707,439

12/15/2003

Li-Wei Shih

AUOP0013USA

1438

27765

7590

12/28/2004

(NAIPC) NORTH AMERICA INTERNATIONAL PATENT OFFICE

P.O. BOX 506

MERRIFIELD, VA 22116

EXAMINER

TRAN, THUY V

ART UNIT

PAPER NUMBER

2821

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,439	SHIH ET AL.	
	Examiner	Art Unit	
	Thuy V. Tran	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>04/14/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is a response to the Applicants' filing on 12/15/2003. In virtue of this filing, claims 1-11 are currently presented in the instant application.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Inventorship

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 04/14/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

4. The drawings submitted on 12/15/2003 are accepted.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-5, 7-9, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Sung (Pub. No.: US 2003/0197665).

With respect to claim 1, Sung discloses, in Fig. 1, a driving circuit and a corresponding driving method comprising the steps of (a) providing a first metal transistor [106] whose first and second ends are connected to an OLED [108] and to a first voltage source [Vss] respectively, (b) providing a capacitor [C] whose first end is connected to a gate of the first MOS transistor [106], (c) providing a second MOS transistor [102] whose first end is utilized for inputting data (from Vdata), a second end of the second MOS transistor [102] being connected to the first end of the capacitor [C], (d) turning on the second MOS transistor [102] and inputting data from the first end of the second MOS transistor to the second end of the second MOS transistor [102], and (e) turning off the second MOS transistor [102] after step (d), and adjusting a voltage [Vref] at a second end of the capacitor [C] from a first voltage level to a second voltage level different from the first voltage level sequentially.

With respect to claims 2-3, Sung discloses, in Fig. 1, that the first voltage level is lower or greater than the second voltage level (see paragraph [0025], lines 1-14).

With respect to claim 4, Sung discloses, in Fig. 1, that the step (e) comprises a step of, after the voltage at the second end of the capacitor [C] has been adjusted to a voltage level equal to the second voltage level, adjusting the voltage at the second end of the capacitor [C] to a voltage level equal to the first voltage level again (see paragraph [0025], lines 1-14).

With respect to claims 5 and 7, Fig. 1 of Sung shows that the first MOS transistor [106] is a thin film transistor (TFT) and that the first transistor [106] is an NMOS transistor.

With respect to claim 8, Sung discloses, in Fig. 1, an OLED driving circuit comprising: (1) an OLED having a first end connected to a first voltage source, (2) a first MOS transistor [106] having a first end connected to a second end of the OLED and a second end connected to a second voltage source, (3) a second MOS transistor [102] having a first end connected to a gate of the first transistor [106], a second end for inputting data (from Vdata), and a gate for inputting a select signal, and (4) a capacitor [C] having a first end connected to the first end of the second MOS transistor and a second end connected to a reference voltage [Vref].

With respect to claims 9 and 11, Fig. 1 of Sung shows that the first MOS transistor [106] is a thin film transistor (TFT) and that the first transistor [106] is an NMOS transistor.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (Pub. No.: US 2003/0197665).

With respect to claims 6 and 10, Sung discloses all of the claimed subject matter, as expressly recited in claims 1 and 8, except for the first MOS transistor being a PMOS transistor. However, this difference is not of patentable merit since both the NMOS and PMOS transistors are operated in the same manner, provide very high input impedance, and consume little static power even though all voltages and currents are reversed. Therefore, to employ a PMOS transistor, instead of an NMOS transistor, for the first MOS transistor in the driving circuit of Sung, upon a particular application or environment of use, would have been deemed obvious to a person skilled in the art.

Citation of relevant prior art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Cok (Pub. No.: US 2002/0171611 A1) discloses a flat panel display device.

Prior art Sato et al. (Pub. No.: US 2002/0140646 A1) discloses a display module.

Prior art Sung (U.S. Patent No. 6,677,713) discloses a driving circuit and method for LED.

Prior art Ting (U.S. Patent No. 6,486,606) discloses a driving circuit and method for OLED.

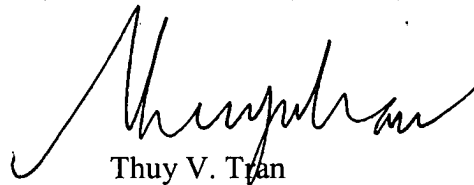
Art Unit: 2821

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuy V. Tran whose telephone number is (571) 272-1828. The examiner can normally be reached on M-F (8:00 AM -5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on (571) 272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thuy V. Tran
Primary Examiner
Art Unit 2821

12/27/2004